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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,722	11/21/2003	Wen-Ting Chu	TS03-373	3171

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EXAMINER	
LINDSAY JR, WALTER LEE	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 12/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/719,722	CHU ET AL.	
	Examiner	Art Unit	
	Walter L. Lindsay, Jr.	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-20* is/are allowed.

6)☒ Claim(s) *1-3,6,8 and 9* is/are rejected.

7)☒ Claim(s) *4,5 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/19/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to an Application filed on 11/21/2003.

Currently, claims 1-20 are pending.

Specification

1. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 8 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakamura et al. (U.S. Patent No. 6,222,225 dated 4/24/2001).

Nakamura shows the method as claimed in Figs. 4A-4B and 5A-5H and corresponding text as: providing a substrate (11) (col. 5, lines 10-19); forming a conductor layer (16a) overlying said substrate with a dielectric layer (15) therebetween (col. 5, lines 10-19); forming a masking layer (31) overlying said conductor layer (col. 5, lines 10-19); forming a resist layer (32) overlying said masking layer (col. 5, lines 20-29); patterning said resist layer to thereby selectively expose said masking layer wherein said resist layer exhibits a first spacing between edges of said resist layer (Fig 5A) (col. 5, lines 20-29); etching through said exposed masking layer to thereby

selectively expose said conductor layer wherein etched edges of said masking layer are tapered such that said masking layer exhibits a second spacing between said masking layer edges at the top surface of said conductor layer and wherein said second spacing is less than said first spacing (Fig. 5B and 5C) (col. 5, lines 20-42); and etching through said exposed conductor layer to thereby complete a transistor gate (col. 5, lines 20-29) (claim 1). Nakamura teaches that the conductor layer comprises polysilicon (col. 5, lines 10-19) (claim 2). Nakamura teaches that the masking layer comprises silicon nitride (col. 5, lines 10-19) (claim 3). Nakamura teaches that the transistor gate is a floating gate of a non-volatile memory device (col. 5, lines 10-19) (claim 8). Nakamura teaches that a control gate is formed overlying the floating gate wherein said control gate (18a) comprises a second conductor layer overlying a second dielectric layer (17); and forming source and drain regions in said substrate (Fig. 4B) (col. 4, lines 39-45)(claim 9).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. (U.S. Patent No. 6,222,225 dated 4/24/2001) in view Lin et al. (U.S. Patent No. 6,673,676 filed 8/27/2002).

Nakamura shows the method substantially as claimed and as described in the preceding paragraphs.

Nakamura lacks anticipation only in not explicitly teaching that: 1) the masking layer comprises a thickness of between about 600 Å and about 4000 Å (claim 6).

Lin teaches in a floating gate processing method, the formation of a silicon nitride masking layer. Lin forms a SiN mask (220) that has a thickness of 500Å to 3000Å (col. 4, lines 20-38), and that is etched to form spaces in between portions of the mask (Fig. 2B) (col.4, lines 39-45). The masking layer is used to overcome problems that occur due to the rapid advancements of the integration of memory such as, the difficulties with alignments in devices calling for finer line widths and improves fabrication of flash memory (col. 2, line 53- col. 3 line 5).

Given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. See In re Aller, Lacey and Hall (10 USPQ 233-237) It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 f.2d 1575,1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

It would be obvious to one of ordinary skill in the art, at the time the invention was made, to modify the method shown in Nakamura by forming a masking layer comprising

a thickness of between about 600Å and about 4000 Å, as taught in Lin, with the motivation that Lin teaches that the masking layer reduces the difficulties with alignments in devices calling for finer line widths and improves fabrication of flash memory.

Allowable Subject Matter

6. Claims 4-5 and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 10-20 are allowed.

8. The following is a statement of reasons for the indication of allowable subject matter: the prior art, either singly or in combination fails to anticipate or render obvious, the limitations of:

...wherein said step of etching through said exposed masking layer comprises a dry etch further comprising an etching chemistry of CFH_3, CF_4, O_2 and He, as required by claim 4;

...wherein the angle of the edges of said masking layer with respect to the top surface of said substrate is between about 45° and about 85°, as required by claim 5;

...forming an isolation region in said substrate wherein said masking layer etched edges overlie said isolation region, as required by claim 7;

...etching through said exposed masking layer thereby selectively expose said conductor layer wherein etched edges of said masking layer are tapered such that said

masking layer exhibits a second spacing between said masking layer edges at the top surface of said conductor layer and wherein said second spacing is less than said first spacing and wherein said masking layer etched edges overlie said isolation region, as required by claim 10 and claim 17.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John F Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walter L. Lindsay, Jr.
Examiner
Art Unit 2812

WLL
December 9, 2004